Amendments to the Claims:

1. (Currently Amended) A logic system for performing scan tests with a single scan clock comprising:

a first clock domain for performing logic operations and scan tests with a first clock signal, the first clock domain including at least one first-domain scan cell for buffering data; and

a second clock domain for performing logic operations with a second clock signal and for performing scan tests with the first clock signal, the second clock domain including at least one second domain scan cell for buffering data.~~;~~

~~wherein when the logic system performs scan tests, the first clock domain and the second clock domain have the clock tree quasi-balance characteristic.~~

2. (Currently Amended) The logic system of claim 1 wherein ~~the first clock domain further comprises at least one first domain scan cell, the~~ first-domain scan cell comprising:

a multiplexer for selectively outputting a function input signal or a scan input signal according to a scan enable signal; and

a D-type flip flop coupled to the multiplexer for receiving and outputting the function input signal or the scan input signal according to the first clock signal.

3. (Currently Amended) The logic system of claim 1 wherein the second clock domain further comprises:

a first multiplexer for selectively outputting the first clock signal or the second clock signal as a second clock domain driving signal according to a mode signal; ~~and~~wherein

~~at least one~~ the second-domain scan cell comprising:

a second multiplexer for selectively outputting a function input signal or a scan input signal according to a scan enable signal; and

a D-type flip flop coupled to the multiplexer for receiving and outputting the function input signal or the scan input signal according to the second clock domain driving signal.

4. (Original) The logic system of claim 1 wherein when performing scan tests, the first clock domain and the second clock domain are linked to form a scan chain.

5. (Currently Amended) The logic system of claim 1 wherein ~~the second clock domain further comprises at least one~~the second-domain scan cell comprising:

a first multiplexer for selectively outputting a function input signal or a scan input signal according to a scan enable signal;

a second multiplexer for selectively outputting the first clock signal or the second clock signal according to a mode signal; and

a D-type flip flop coupled to the first multiplexer and the second multiplexer for receiving and outputting the function input signal or the scan input signal according to the first clock signal or the second clock signal.

6. (Currently Amended) A method for performing scan tests of a logic system, the logic system comprising a multiple clock domain scan test circuit having a first clock domain and a second clock domain, the first clock domain including at least one first-domain scan cell, the second clock domain including at least one second-domain scan cell, the method comprising:

when the logic system performs logic operations, performing logic operations according to a first clock signal and a second clock signal in the first clock domain and the second clock domain respectively; and

when the logic system performs scan tests, performing scan tests according

to a test clock signal in both the first clock domain and the second clock domain so that the first clock domain and the second clock domain demonstrate~~have the~~ clock tree balance characteristic or clock tree quasi-balance characteristic.

7. (Original) The method of claim 6, wherein the test clock signal is the first clock signal.

8-9. (Canceled)

10. (New) A method for performing scan tests in a logic system, the logic system comprising a first clock domain and a second clock domain, the method comprising:

providing a mode signal, the value of which indicates a first mode or a second mode;

operating the first clock domain referencing to a first clock signal during the first mode;

operating the second clock domain referencing to a second clock signal being of a frequency different from a frequency of the first clock signal during the first mode;

operating the first clock domain referencing to the first clock signal to perform a scan test in the first clock domain during the second mode; and

operating the second clock domain referencing to the first clock signal to perform the scan test in the second clock domain during the second mode.

11. (New) The method of claim 10, wherein the logic system further comprising a third clock domain, the method further comprising:

operating the third clock domain referencing to a third clock signal being of a frequency different from a frequency of the first clock signal or a frequency of the second clock signal during the first mode; and

operating the third clock domain referencing to the first clock signal to perform

the scan test in the third clock domain during the second mode.

12. (New) The method of claim 10, further comprising:

providing at least one first-domain scan cell in the first clock domain;

providing at least one second domain scan cell in the second clock domain;

clocking the first-domain scan cell with the first clock signal during the first mode;

clocking the second domain scan cell with the second clock signal during the first mode;

clocking the first-domain scan cell with the first clock signal during the second mode; and

clocking the second-domain scan cell with the first clock signal during the second mode.

13. (New) The method of claim 12, further comprising:

achieving clock tree balance characteristic or clock tree quasi-balance characteristic among the at least one first-domain scan cell and the at least one second-domain scan cell.

14. (New) The method of claim 10, further comprising:

linking the first clock domain and the second clock domain to form a single scan chain during the second mode.

15. (New) The method of claim 14, wherein the scan chain comprises the at least one first-domain scan cell and the at least one second-domain scan cell.